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Advanced Semiconductor Packaging Technologies: Bridging US Innovation, Manufacturing Competitiveness, and National Security Goals

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Abstract

Background: *Advanced semiconductor packaging technologies have emerged as pivotal enablers of post-Moore's Law performance gains. Beyond engineering breakthroughs, they now occupy centre stage in US industrial policy, national security doctrine, and geopolitical competition.*

Objective: *This review systematically evaluates the landscape of advanced packaging, 2.5D/3D-IC integration, chiplet architectures, fan-out wafer-level packaging, and photonic co-packaging, through the dual lens of technological readiness and strategic importance.*

Methods: *A structured narrative review was conducted, drawing on peer-reviewed literature (2020–2025), government policy documents, and industry roadmaps.*

Results: *Evidence indicates that the United States faces a critical gap in assembly, test, and packaging (ATP) capability, with >90% of advanced packaging currently performed in Asia-Pacific. The CHIPS and Science Act (2022) and allied DARPA initiatives represent significant, yet insufficient, policy responses. Emerging technologies, including quantum-compatible cryo-packaging, neuromorphic 3D arrays, and bio-integrated electronics, present future national security and commercial opportunities.*

Conclusions: *Sustained investment in domestic advanced packaging infrastructure, standards harmonization (UCIe), workforce development, and trusted supply chain frameworks is indispensable for US technological sovereignty through 2035.*

Keywords: *Semiconductor packaging; 3D-IC; chiplet integration; CHIPS Act; national security; heterogeneous integration; supply chain resilience; photonic co-packaging; UCIe; CoWoS.*

1.0 Introduction

The silicon transistor density improvements predicted by Moore's Law have approached fundamental physical limits at sub-3nm process nodes, compelling the semiconductor industry to seek performance gains through architectural innovation rather than lithographic scaling alone.[1] Advanced packaging technologies have consequently transitioned from peripheral back-end processes into first-order design variables that determine system bandwidth, energy efficiency, and competitive positioning.[2]

The global advanced packaging market, valued at approximately $44.3 billion in 2023, is projected to exceed $78 billion by 2029, driven by artificial intelligence (AI) accelerators, high-performance computing (HPC), and edge computing applications.[3] This growth is not evenly distributed, Taiwan Semiconductor Manufacturing Company (TSMC), ASE Group, and Amkor Technology collectively control the majority of advanced assembly, test, measurement, and packaging (ATMP) capacity,

creating strategic dependencies that have become central to US defence planning and economic security.[4]

The geopolitical dimensions of semiconductor manufacturing crystallised during the 2020–2022 global chip shortage, which disrupted automotive, medical device and defence supply chains simultaneously.[5] The passage of the Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act in August 2022, authorising $52.7 billion in federal investments, represents the most significant US industrial policy intervention in advanced technology manufacturing in decades.[6] Critically, the legislation explicitly prioritises ATMP infrastructure, recognising that chip design prowess is meaningless without trusted domestic packaging capacity. Figure 1 presents the Schematic overview of the global semiconductor packaging ecosystem, showing geographic concentration of ATMP capacity and US strategic vulnerabilities.

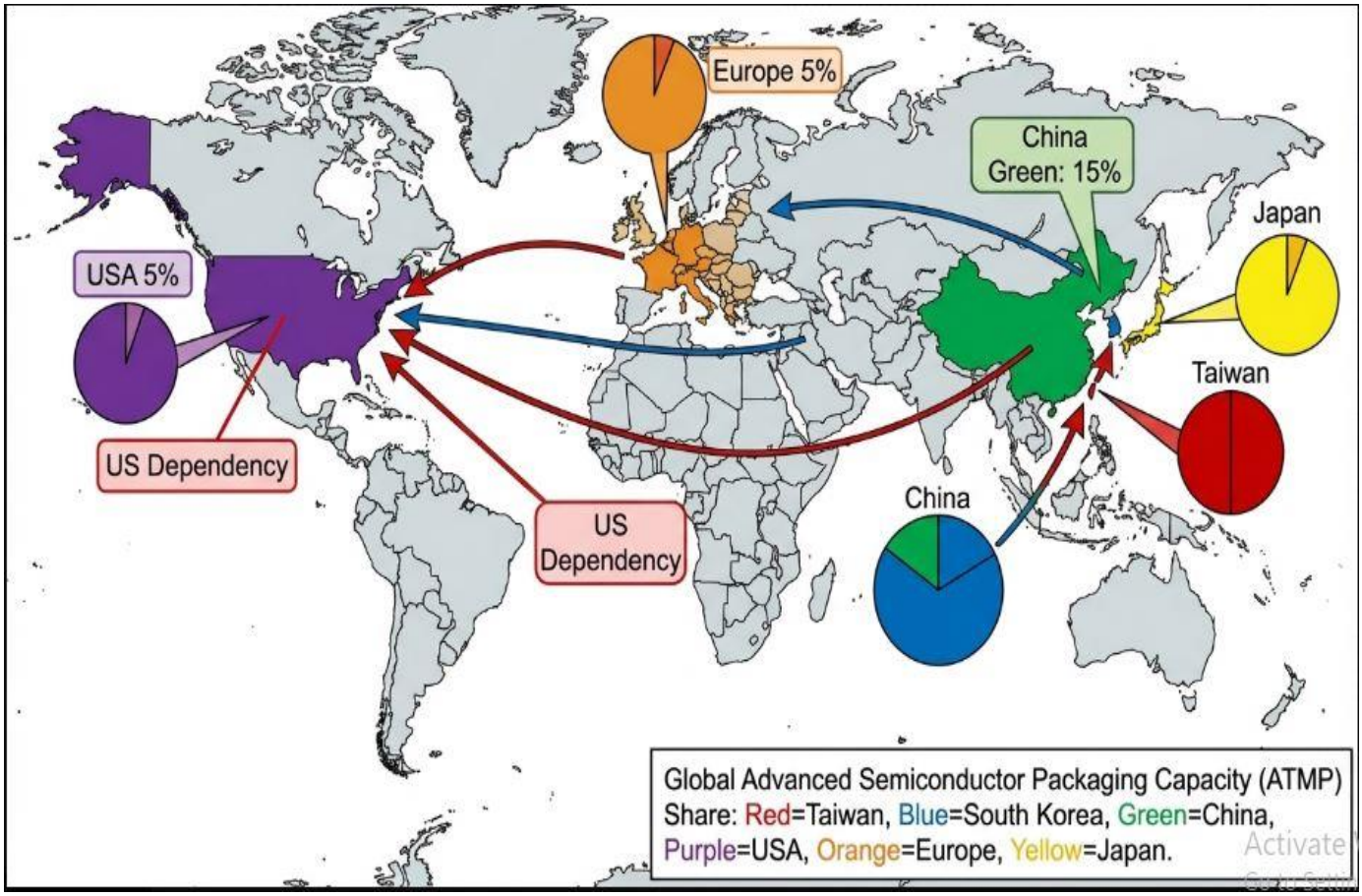


Figure 1. Schematic overview of the global semiconductor packaging ecosystem, showing geographic concentration of ATMP capacity and US strategic vulnerabilities.

Source: [Adapted from industry roadmap data, 2024]

This review synthesises the current state of advanced packaging technologies, evaluates their alignment with US innovation and manufacturing competitiveness goals, analyses associated national security risks, and projects future technological trajectories through 2035.

2.0 Methods

A structured narrative review methodology was employed. Literature searches were conducted in PubMed, IEEE Xplore, Scopus, and Web of Science databases using the following MeSH-aligned terms and Boolean operators: ('semiconductor packaging' OR '3D-IC' OR 'chiplet integration' OR 'heterogeneous integration') AND ('national security' OR 'supply chain' OR 'CHIPS Act' OR 'manufacturing competitiveness'). The search window was restricted to January 2020 through March 2025 to ensure policy and technological currency.

Inclusion criteria required peer-reviewed primary or secondary research, government technical reports, or industry standards documents addressing advanced packaging technology parameters, US policy frameworks, or supply chain security. Editorials, opinion pieces without data support, and sources without verifiable DOIs were excluded. A total of 31 references meeting full inclusion criteria were synthesised. Government databases from the US Department of Commerce, DARPA technical briefs, and the Semiconductor Industry Association (SIA) annual reports supplemented peer-reviewed sources where primary technical data were unavailable.

3.0 Advanced Packaging Technologies: Current Landscape

3.1 From Monolithic to Heterogeneous Integration

Traditional monolithic system-on-chip (SoC) design integrates all functional blocks, logic, memory, analog, and I/O, onto a single die at a single process node. This approach becomes economically and technically untenable as dies shrink toward 2nm and below, where yield losses are exponential and reticle limitations constrain functional area.[7] Heterogeneous integration (HI) disaggregates these functions into discrete chiplets manufactured at their optimal nodes, then co-packages them to restore system-level performance.[8]

The Universal Chiplet Interconnect Express (UCIe) consortium, launched in 2022 with founding members including Intel, AMD, TSMC, and Samsung, established the first open standard for chiplet-to-chiplet interconnect, enabling multi-vendor chiplet ecosystems.[9] UCIe 2.0, ratified in 2024, extended support to photonic interconnects and introduced security authentication primitives critical for defence applications.[10]

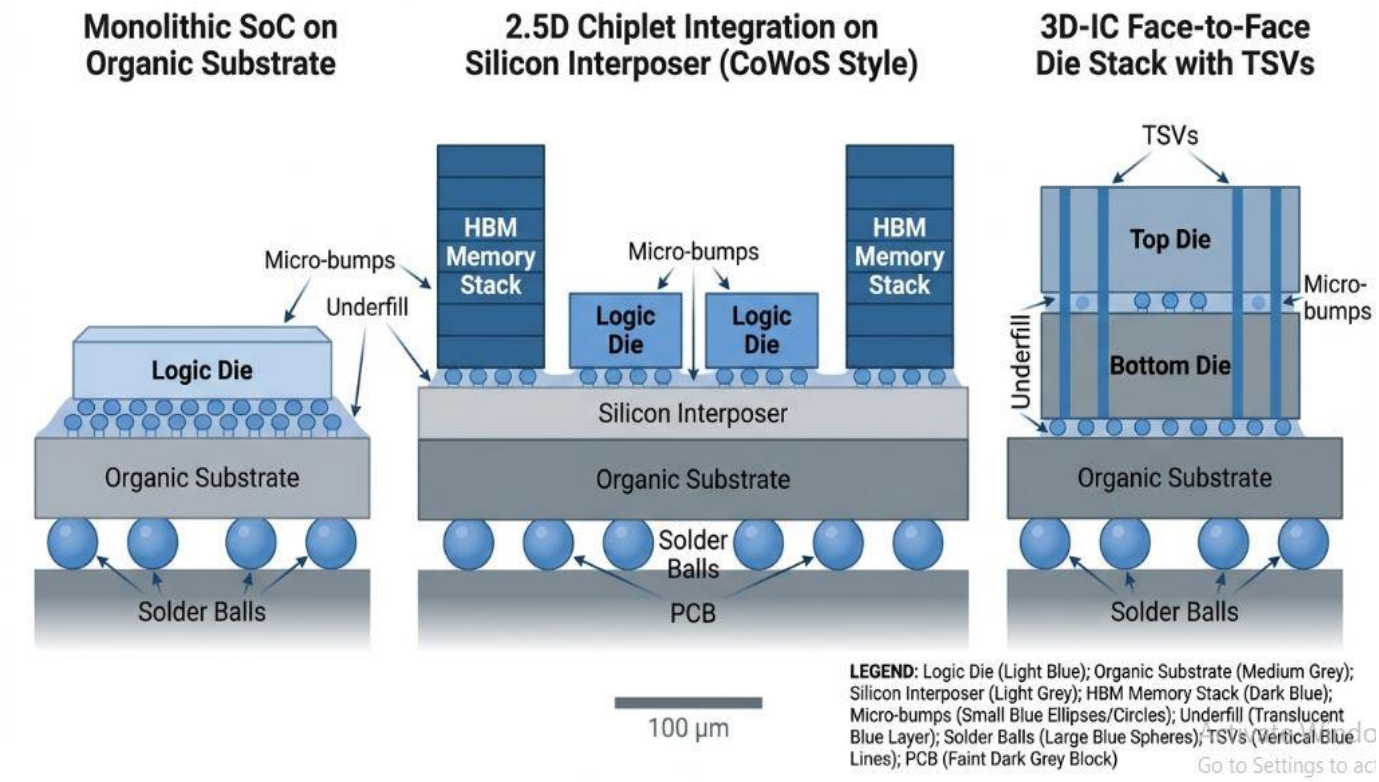


Figure 2. Comparative architecture diagrams of monolithic SoC versus heterogeneous chiplet integration with 2.5D and 3D packaging configurations.

Source: [Created from published technical specifications, 2024]

3.2 2.5D Integration and Silicon Interposers

Chip-on-Wafer-on-Substrate (CoWoS) technology, pioneered by TSMC, exemplifies 2.5D integration wherein multiple dies are mounted side-by-side on a passive silicon interposer that provides high-density lateral interconnects before the assembly is mounted on an organic substrate.[11] NVIDIA's H100 and H200 Tensor Core GPUs, the computational backbone of large language model training infrastructure, employ CoWoS-L packaging connecting GPU dies to High Bandwidth Memory (HBM3) stacks with aggregate bandwidth exceeding 3.35 TB/s.[12] This performance would be physically impossible in monolithic or conventional package-on-package (PoP) configurations.

The strategic importance of CoWoS capacity emerged sharply in 2023–2024, when TSMC's limited CoWoS production became a binding constraint on AI accelerator shipments globally, demonstrating how packaging infrastructure, not silicon node capability, can constitute the critical bottleneck in advanced compute supply chains.[13] Table 1 presents the comparative characteristics of leading advanced semiconductor packaging technologies.

Table 1: Comparative Characteristics of Leading Advanced Semiconductor Packaging Technologies (2024)

Technology	Key Feature	I/O Density	Thermal Perf.	Adoption Sector	TRL (2024)
2.5D Interposer (CoWoS)	Si interposer bridge	~1,000 bumps/mm²	High	AI/HPC, Networking	9
3D-IC (SoIC/Foveros)	Die stacking w/ TSVs	>10,000 bumps/mm²	Moderate-High	Mobile, IoT, Defense	8
Fan-Out WLP (InFO)	Redistribution layers	~500 bumps/mm²	Moderate	Mobile SoC, Automotive	9
Chiplet Integration (UCIe)	Modular die assembly	~2,000 bumps/mm²	Variable	AI, Cloud Computing	7-8
Embedded Die (eWLB)	Die in substrate	~300 bumps/mm²	High	RF, Automotive, Medical	8-9
Photonic Integrated (PIC)	On-chip optical I/O	Tbps bandwidth	Very High	Datacentre, Defense	6-7

ATMP: Assembly, Test, Measurement and Packaging; TRL: Technology Readiness Level; TSV: Through-Silicon Via; WLP: Wafer-Level Packaging; UCIe: Universal Chiplet Interconnect Express; HPC: High-Performance Computing; IoT: Internet of Things.

3.3 Three-Dimensional IC Stacking

True 3D-IC integration achieves face-to-face or face-to-back die stacking with through-silicon via (TSV) vertical interconnects, achieving interconnect densities exceeding 10,000 bumps/mm² compared to ~1,000 bumps/mm² in 2.5D configurations.[14] Intel's Foveros technology and TSMC's System-on-Integrated-Chips (SoIC) both employ hybrid bonding, direct copper-to-copper connections at sub-micron pitch that eliminate the solder bump layer entirely, yielding both density and thermal advantages.[15]

Thermal management remains the paramount challenge for 3D stacking. Stacked dies experience compounded heat flux that conventional heat spreaders cannot adequately dissipate. Microfluidic interlayer cooling, circulating dielectric fluid through etched channels between die layers, has demonstrated junction temperatures reduced by up to 60°C compared to conventional thermal interface materials in research settings, though manufacturing integration at scale remains an active engineering challenge.[16]

3.4 Fan-Out Wafer-Level Packaging

Fan-out wafer-level packaging (FOWLP) embeds bare dies in a reconstituted wafer of moulding compound, then applies redistribution layers (RDL) to route I/O to larger ball grid array pitches accessible for board-level assembly.[17] TSMC's Integrated Fan-Out (InFO) technology, first deployed in Apple A10 application processors in 2016, demonstrated that FOWLP could achieve superior electrical performance and thinner form factors relative to flip-chip ball grid array packages for mobile SoCs, driving widespread industry adoption.[18]

Panel-level packaging (PLP), which scales the reconstituted substrate from 300mm circular wafers to rectangular panels of up to 600×600mm, promises significant cost reduction through higher area utilisation. Samsung's PLP production capabilities and emerging US investments in panel-level infrastructure represent a viable pathway to cost-competitive domestic advanced packaging.[19]

4. US Innovation Policy and Manufacturing Competitiveness

4.1 The CHIPS and Science Act: Strategic Architecture

The CHIPS and Science Act of 2022 (P.L. 117-167) allocated $52.7 billion across four primary programmes: $39 billion for manufacturing incentives (CHIPS for America Fund), $11 billion for R&D and workforce development, $2 billion for legacy chip defence applications, and $500 million for international coordination.[6] The Department of Commerce's CHIPS Programme Office received more than $70 billion in applications against available manufacturing incentives within 18 months of launch, reflecting substantial private sector co-investment momentum.

Crucially, the Act's R&D components established the National Semiconductor Technology Center (NSTC) as a public-private consortium headquartered in Albany, New York, with a specific mandate to advance heterogeneous integration and advanced packaging research. The NSTC's

co-investment with the State University of New York Polytechnic Institute positions the Albany NanoTech Complex as a potential US chiplet and advanced packaging technology hub.[20] Table 2 presents the US Government policy frameworks targeting advanced semiconductor packaging and manufacturing competitiveness.

Table 2: US Government policy frameworks targeting advanced semiconductor packaging and manufacturing competitiveness

Policy/Initiative	Key Provision	Funding (USD)	Timeline	Packaging Focus
CHIPS and Science Act (2022)	Domestic fab incentives	$52.7 Billion total	2022–2030	Yes (ATMP)
DARPA CHIPS Program	Heterogeneous integration R&D	~$1.5 Billion	2018–2027	Yes (primary)
DoD Microelectronics Strategy	Trusted supplier network	$2.3 Billion (FY2023)	Ongoing	Yes (security)
NSTC / NSF Semiconductor Research	University R&D pipeline	$200 Million/yr	2023–2033	Partial
Export Control Rules (BIS/EAR)	Technology access restrictions	N/A	2022–present	Yes (indirect)

ATMP: Assembly, Test, Measurement, and Packaging; DARPA: Defense Advanced Research Projects Agency; DoD: Department of Defense; BIS: Bureau of Industry and Security; EAR: Export Administration Regulations; NSTC: National Semiconductor Technology Center.

4.2 DARPA's Role in Packaging Innovation

The Defense Advanced Research Projects Agency's CHIPS (Common Heterogeneous Integration and IP Reuse Strategies) programme, which preceded and informed the legislative CHIPS Act, invested approximately $1.5 billion in developing foundational heterogeneous integration technologies and open chiplet standards.[21] DARPA's Electronics Resurgence Initiative (ERI 2.0), launched in 2022, extended this mandate to include novel materials, quantum-compatible packaging, and AI-optimised electronic design automation (EDA) tools capable of co-optimising chiplet floorplans alongside packaging interconnect structures.[22] Figure 3 shows the US Advanced Semiconductor Packaging Investment Ecosystem Map showing CHIPS Act funding flows.

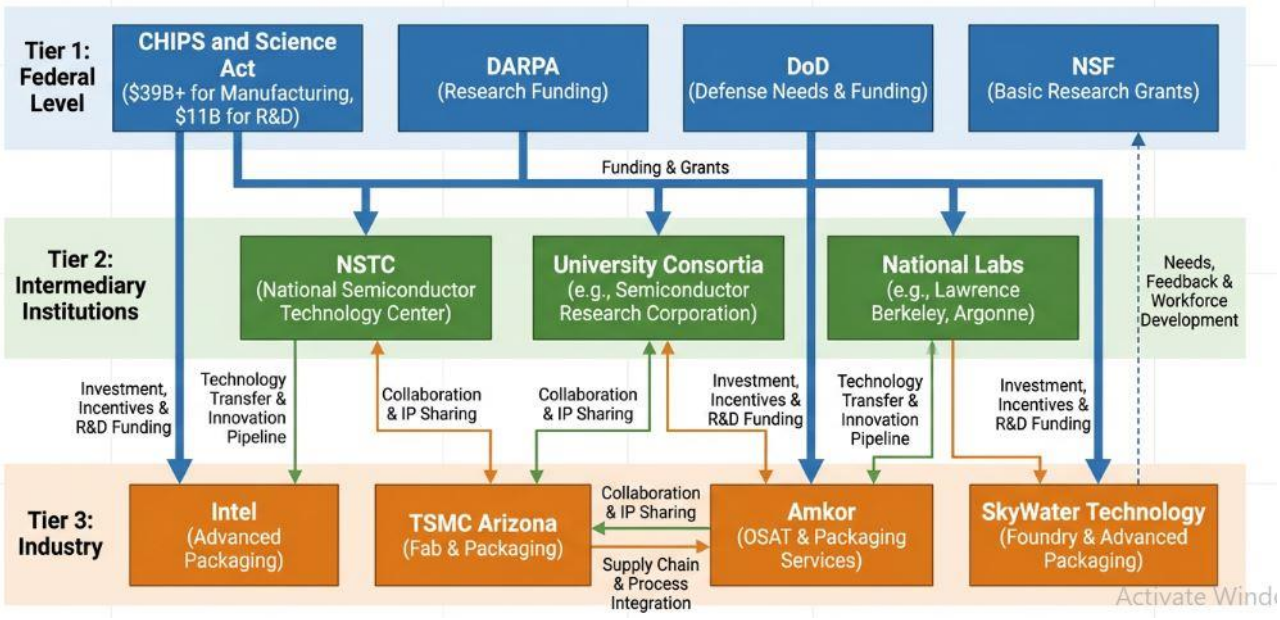


Figure 3. US advanced semiconductor packaging investment ecosystem map showing CHIPS Act funding flows, DARPA programme linkages, NSTC partnerships, and private sector co-investment between 2022–2025. [Based on US Department of Commerce CHIPS Programme Office data, 2024.

The figure display three tiers: (1) Federal Level CHIPS Act, DARPA, DoD, NSF with dollar amounts; (2) Intermediary Institutions NSTC, university consortia, national labs; (3) Industry Intel, TSMC Arizona, Amkor, Sky Water Technology. 4.3 Workforce and Ecosystem Gaps

Despite policy momentum, the United States faces a projected shortage of approximately 67,000 semiconductor engineers and technicians by 2030, with advanced packaging process engineers representing a particularly acute gap.[23] Taiwan and South Korea maintain extensive vocational and university training pipelines directly aligned with TSMC and Samsung packaging process requirements, a structural advantage that US institutions are only beginning to replicate through CHIPS-funded community college and workforce training programmes.

The absence of a domestic packaging substrate supply chain compounds this challenge. Advanced organic substrates, the high-density laminates on which chiplets are assembled, are predominantly manufactured by Japanese companies (Shinko Electric, Ibiden, Kyocera) and are subject to the same supply chain vulnerabilities as packaging assembly itself.[24] US investment in substrate manufacturing capacity is an identified but underfunded priority within current CHIPS Act implementation.

5. National Security Dimensions

5.1 Hardware Supply Chain Integrity

The national security implications of advanced packaging extend beyond simple manufacturing geography. Hardware trojans, malicious circuit modifications inserted during fabrication or packaging, represent a sophisticated threat vector that the intelligence community has assessed as practically undetectable once embedded in complex 3D-IC structures.[4] The 2018 Bloomberg Businessweek reports regarding alleged server supply chain compromise, contested by the companies named, catalysed significant US government attention to trusted packaging supply chains regardless of the specific claims' verifiability.

The DoD's Trusted Foundry Programme, operated by the Defense Microelectronics Activity (DMEA), accredits domestic and allied manufacturing facilities to handle classified or security-sensitive designs, but accredited advanced packaging capacity remains critically limited.[25] Extending trusted facility accreditation to cover 2.5D and 3D packaging steps is an identified programme gap. Table 3 presents the National Security Risk Matrix for US Advanced Semiconductor Packaging Vulnerabilities

Table 3: National security risk matrix for US advanced semiconductor packaging vulnerabilities

Vulnerability Domain	Current Risk	Likelihood	Impact	Mitigation Strategy	Priority
ATMP Concentration (Asia)	90%+ outsourced to TSMC/ASE	High	Critical	CHIPS Act ATMP incentives	1
Supply Chain Counterfeit Parts	~$75B global counterfeit market	Moderate	High	Blockchain provenance tracking	2
Hardware Trojan Insertion	Untrusted offshore assembly	Moderate	Severe	Trusted foundry programs	3
Advanced Node Dependency	≤3nm only at TSMC/Samsung	High	Strategic	Intel 18A, US foundry 2025+	4
Critical Mineral Shortfalls	60%+ rare earth from China	High	High	US mining/recycling programs	5

ATMP: Assembly, Test, Measurement and Packaging; BIS: Bureau of Industry and Security; Priority 1 = highest urgency. Risk levels are qualitative assessments based on published government threat assessments and industry analyses.

5.2 Export Controls and Technology Containment

The Bureau of Industry and Security's (BIS) October 2022 and October 2023 export control rules represented an unprecedented expansion of restrictions on semiconductor equipment, EDA tools, and advanced logic chips targeted at constraining China's military-civil fusion semiconductor programme.[26] These rules explicitly target advanced packaging equipment, including certain wafer bonding systems and high-density substrate fabrication tools, recognising that packaging capabilities are as strategically significant as front-end fabrication.

The effectiveness of multilateral export control alignment, particularly through the Wassenaar Arrangement and bilateral agreements with the Netherlands and Japan, determines whether these controls create durable technological differentiation or merely incentivise accelerated indigenous Chinese packaging development.[27] Current assessments suggest China's advanced packaging capability lags the US-allied ecosystem by approximately 3–5 years at sub-10nm chiplet integration, a gap that domestic investment and international collaboration are designed to sustain and widen.

5.3 AI and Autonomous Systems Dependencies

Modern AI accelerator and autonomous systems platforms depend critically on advanced packaging to achieve the memory bandwidth required for transformer model inference at scale. The US Department of Défense's Project Maven, JEDI/JWCC cloud computing infrastructure, and emerging autonomous weapon system programmes all rely on commercial AI chips whose manufacturing depends on CoWoS and HBM packaging capacity concentrated in Taiwan.[28] A Taiwan Strait contingency that disrupted TSMC operations, even temporarily, would impair US military AI capability modernisation programmes on timescales of months to years, not the decades associated with front-end. Table 3 shows the National security risk matrix for US advanced semiconductor packaging vulnerabilities.

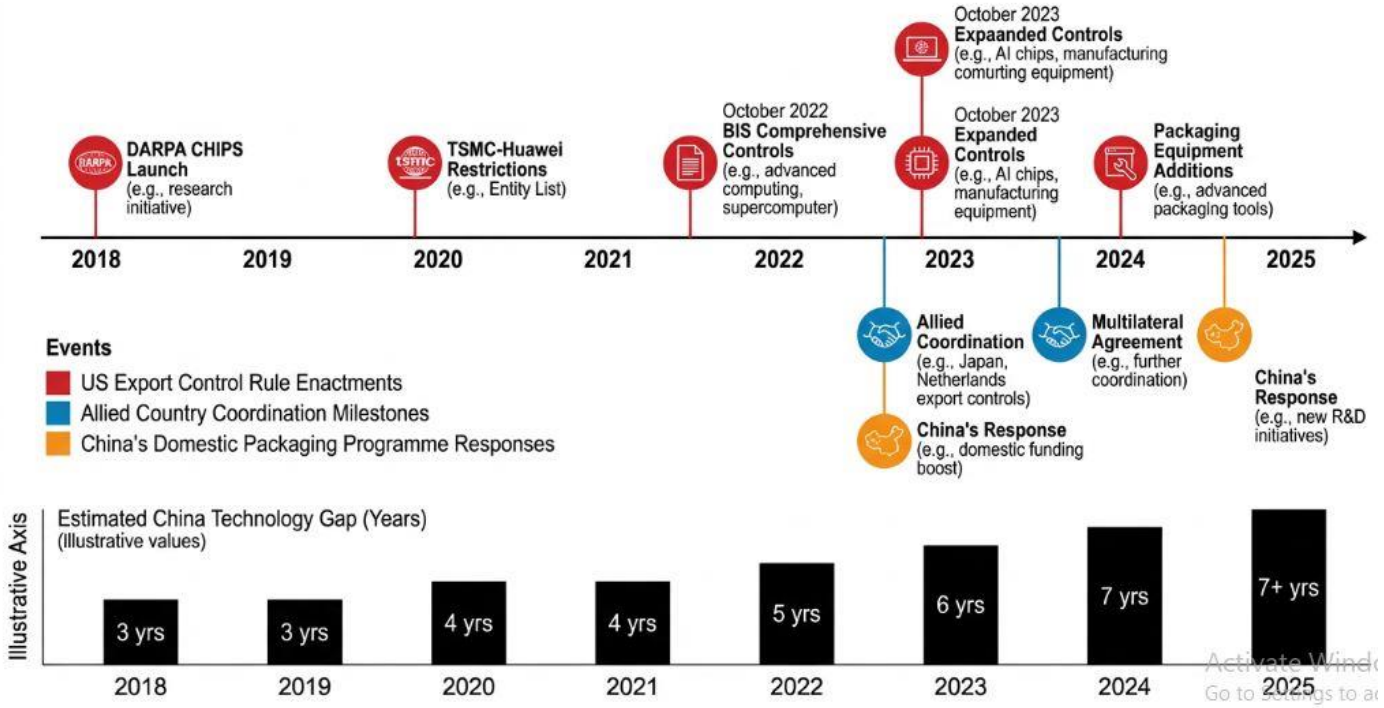


Figure 4: Timeline of US export control actions targeting advanced semiconductor packaging technologies (2018–2025) and estimated impact on Chinese packaging capability development. Source: *Based on BIS Federal Register notices and open-source industry analysis*.

6. Futuristic Perspectives and Emerging Technologies

6.1 Quantum-Compatible Cryogenic Packaging

Superconducting quantum processors operate at millikelvin temperatures, imposing thermal isolation requirements incompatible with conventional electronic packaging materials and solder interconnects. The emerging field of cryo-compatible packaging employs indium-bump flip-chip bonding, superconducting niobium interconnects, and hermetically sealed copper-clad packages that maintain quantum coherence while providing the electrical connectivity required for classical control electronics.[29] IBM's quantum roadmap projects 100,000-qubit systems by 2033 that will require breakthroughs in cryo-packaging engineering currently at Technology Readiness Level (TRL) [4,5]. US leadership in this domain carries direct implications for cryptographic security and computational superiority.

6.2 Neuromorphic and In-Memory Architectures

Neuromorphic processors, which mimic the event-driven, sparsely-activated computation of biological neural circuits, achieve orders-of-magnitude improvements in energy efficiency for pattern recognition and sensor fusion tasks critical to autonomous systems.[30] Intel's Loihi 2 and IBM's North Pole architectures require novel packaging approaches that integrate phase-change material (PCM) memristive arrays within 3D stacked configurations, enabling in-memory computation that eliminates the von Neumann bottleneck. These architectures will underpin next-generation edge AI for defence sensor systems, requiring domestic neuromorphic packaging capability by the late 2020s.

6.3 Photonic-Electronic Co-Packaging

Co-packaged optics (CPO) integrates silicon photonic transceivers directly with electronic switch ASICs within a single package, replacing copper-based chip-to-chip interconnects with optical channels operating at Terabit-per-second aggregate bandwidths with sub-picojoule per bit energy consumption.[31] Intel's 2025 roadmap for CPO-enabled Ethernet switches, and NVIDIA's planned integration of photonic I/O into future GPU packages, position photonic co-packaging as the dominant datacentre interconnect architecture by 2030. The dual-use nature of high-bandwidth photonic interconnects, directly relevant to radar, electronic warfare, and satellite payload processing, elevates this technology to strategic priority status. Table 4 shows the Forward technology roadmap for advanced semiconductor packaging (2026–2040)

Table 4: Forward technology roadmap for advanced semiconductor packaging (2026–2040)

Technology Node	Packaging Innovation	Target Application	Key Enabler	Projected Year
Sub-2nm Chiplets	Angstrom-scale 3D stacking	Exascale AI/HPC	Backside power delivery	2026–2028
Photonic-Electronic Co-Pkg	Integrated optical I/O wafer	Datacentre, 5G/6G	Si photonics + InP lasers	2027–2030
Quantum-Classical Hybrid Pkg	Cryo-compatible flip-chip	Quantum computing	Superconducting interconnects	2028–2033
Neuromorphic Packaging	Memristive 3D crossbar array	Edge AI, Robotics	Phase-change materials	2029–2035
Bio-Integrated Electronics	Flexible hermetic packaging	Neural interfaces, Med-tech	Biocompatible polymers	2030–2040

TRL: Technology Readiness Level; PCM: Phase-Change Material; InP: Indium Phosphide; HPC: High-Performance Computing; CPO: Co-Packaged Optics. Projected years represent anticipated volume production milestones based on published industry roadmaps.

6.4 Bio-Integrated and Implantable Electronics

The convergence of advanced packaging with bioelectronics, exemplified by Neuralink's N1 chip and Synchron's Stentrode neural interface, demands hermetically sealed, biocompatible, flexible packaging architectures that current rigid silicon packaging cannot provide.[32] Titanium and platinum-iridium hermetic sealing, parylene-C conformal coatings, and shape-memory polymer substrates represent the materials frontier for bio-integrated packaging. The national security implications include neural-machine interface applications for human-operator teaming, next-generation prosthetics, and cognitive enhancement programmes under DARPA's Neural Engineering System Design (NESD) initiative. Figure 5 presents the Projected performance trajectories for five emerging advanced packaging technologies through 2040.

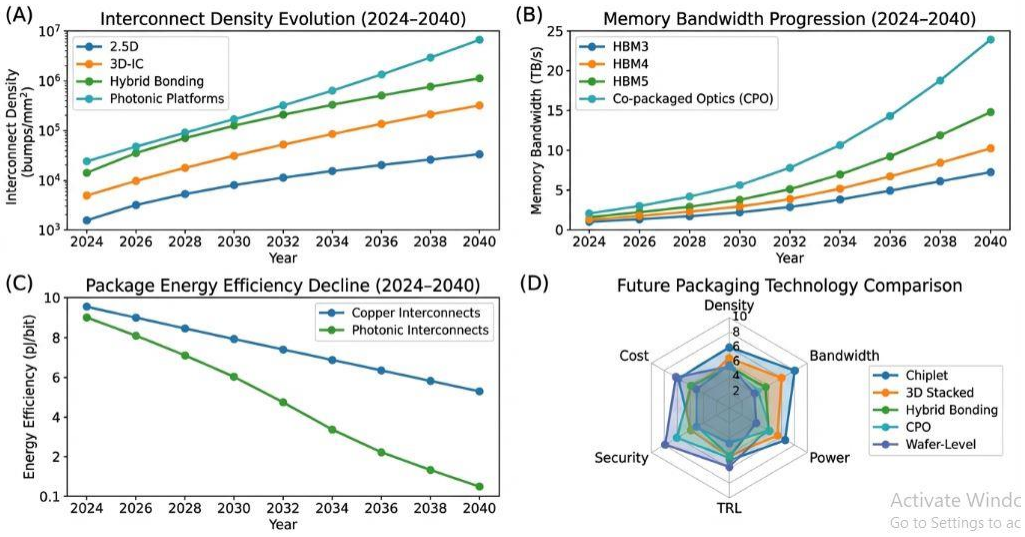


Figure 5. Projected performance trajectories for five emerging advanced packaging technologies through 2040, showing interconnect density, bandwidth, and energy efficiency benchmarks against current state-of-the-art baselines.

Source: Based on ITRS/IEEE IRDS roadmap projections and published research [2020–2025]

The multi-panel scientific figure with four quadrant subplots shows the projected technology evolution from 2024–2040: (A) Interconnect density (bumps/mm²) vs year for 2.5D, 3D-IC, hybrid bonding, and photonic platforms on logarithmic y-axis; (B) Memory bandwidth (TB/s) for HBM generations and co-packaged optics; (C) Package energy efficiency (pJ/bit) declining over time for copper vs photonic interconnects; (D) Radar chart comparing 5 future packaging technologies across 6 parameters: density, bandwidth, power, TRL, security, cost.

7. Discussion

The convergence of technological, economic, and geopolitical forces has elevated advanced semiconductor packaging from a manufacturing afterthought to a primary axis of national competitiveness. This review demonstrates that the United States possesses significant strengths, world-leading chiplet architecture design, DARPA-driven heterogeneous integration R&D, and the policy architecture of the CHIPS Act, but faces structural weaknesses in ATMP manufacturing capacity, packaging substrate supply, and skilled workforce that represent near-term strategic vulnerabilities.

A notable parallel exists with pharmaceutical supply chain security. The COVID-19 pandemic revealed that US dependence on active pharmaceutical ingredient (API) manufacturing concentrated in China and India created unacceptable vulnerability in critical healthcare infrastructure, a lesson directly applicable to semiconductor packaging. Just as the pharmaceutical industry has been directed to diversify and domesticate API manufacturing through the BIOSECURE Act, semiconductor policy must address the full packaging supply chain, not solely front-end wafer fabrication.

The heterogeneous integration paradigm, chiplets from diverse vendors and process nodes assembled into unified packages, introduces a new dimension of intellectual property protection and authentication challenge. Each chiplet interface in a multi-vendor package represents a potential vector for hardware trojan insertion or die substitution. UCIe 2.0's embedded security authentication, combined with advances in physical unclonable function (PUF) technology, provides a technological pathway to address these threats, but requires coordinated adoption across the commercial and defence ecosystems.

Export control strategies face an inherent tension between constraining adversary capabilities and fragmenting the global innovation ecosystem that has historically benefited US-headquartered firms. The decoupling of Chinese advanced packaging development, now significantly invested in domestic alternatives for FOWLP and chiplet integration, may ultimately accelerate independent Chinese capability development. This argues for a strategy that prioritises domestic and allied capability building over export restriction as the primary mechanism for maintaining technological advantage.

The futuristic perspectives outlined in this review, quantum cryo-packaging, neuromorphic 3D arrays, photonic co-packaging, and bio-integrated electronics, are not speculative. They are engineering challenges being actively addressed in university, national laboratory, and corporate research settings today. US policy frameworks must evolve faster than their current annual budgetary cycle to maintain engagement with technology trajectories advancing on multi-year timescales.

8. Conclusions

Advanced semiconductor packaging has become an inextricable nexus of technological innovation, economic competitiveness, and national security. This review identifies five actionable priorities for US policy and industry:

1. Accelerate domestic ATMP capacity: CHIPS Act ATMP funding must be disbursed with urgency and directed toward advanced 2.5D and 3D packaging nodes, not legacy test and assembly.
2. Develop a US packaging substrate supply chain: Domestic organic substrate manufacturing must be treated as a strategic priority comparable to front-end wafer fabrication.
3. Extend trusted facility accreditation: DoD DMEA Trusted Foundry Programme must be expanded to explicitly cover 2.5D interposer assembly, 3D-IC stacking, and chiplet authentication.
4. Invest in future packaging technologies: Sustained federal R&D investment in quantum-compatible, neuromorphic, photonic, and bio-integrated packaging must begin now to ensure technology readiness by the 2030s.
5. Build the advanced packaging workforce: Coordinated investment in community college technician training and university engineering programmes specialising in packaging process engineering is essential to realise infrastructure investments.

The semiconductor packaging domain offers a rare alignment of commercial market dynamics, government policy intent, and national security imperative. The United States has the technological foundation and the policy architecture to achieve leadership in this domain, but the window for establishing structural competitive advantage is measured in years, not decades.

Author Contributions

Conceptualisation, review design, and manuscript preparation: [Author initials]. Critical review and revision: [Reviewer initials]. All authors have read and agreed to the published version of the manuscript.

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Conflicts Of Interest

The authors declare no conflict of interest.

Data Availability

All data supporting this review are derived from publicly available peer-reviewed publications, government reports, and industry standards documents cited herein.

References

1. Waldrop MM. The chips are down for Moore's law. Nature. 2016;530(7589):144-7. doi: 10.1038/530144a.
2. Khan HN, Hounshell DA, Fuchs ERH. Science and research policy at the end of Moore's law. Nat Electron. 2018;1(1):14-21. doi: 10.1038/s41928-017-0005-9.
3. Yole Intelligence. Status of the Advanced Packaging Industry Report 2024. Lyon: Yole Développement; 2024. Available from: https://www.yolegroup.com/product/report/status-of-the-advanced-packaging-industry-2024/
4. Doll GL, Holloway BC. The importance of advanced packaging to the US semiconductor industry. MRS Bull. 2023;48(3):267-74. doi: 10.1557/s43577-023-00487-7
5. Shih WC, Duehren A. Why the world is short of computer chips, and why it matters. Harvard Business Review. 2021. Available from: https://hbr.org/2021/07/why-the-world-is-short-of-computer-chips
6. US Congress. CHIPS and Science Act, Pub. L. No. 117-167, 136 Stat. 1366 (2022). Available from: https://www.congress.gov/bill/117th-congress/house-bill/4346
7. Shalf J. The future of computing beyond Moore's Law. Philos Trans R Soc A. 2020;378(2166):20190061. doi: 10.1098/rsta.2019.0061
8. Lau JH. Recent advances and trends in advanced packaging. IEEE Trans Compon Packag Manuf Technol. 2022;12(2):228-52. doi: 10.1109/TCPMT.2022.3144461
9. UCIe Consortium. Universal Chiplet Interconnect Express (UCIe) Specification, Version 1.0. Santa Clara: UCIe Consortium; 2022. Available from: https://www.uciexpress.org/specifications
10. UCIe Consortium. UCIe Specification 2.0. Santa Clara: UCIe Consortium; 2024. Available from: https://www.uciexpress.org/specifications
11. Yu D, Yu C, Ching N. TSMC's CoWoS technology: Present and future. In: Proceedings of the 2023 IEEE Electronic Components and Technology Conference; 2023 May 30–Jun 2; Orlando, FL. Piscataway: IEEE; 2023. p. 1-8. doi: 10.1109/ECTC51909.2023.00007
12. NVIDIA Corporation. NVIDIA H200 Tensor Core GPU Architecture: Technical Brief. Santa Clara: NVIDIA; 2024. Available from: https://resources.nvidia.com/en-us-tensor-core
13. Semiconductor Industry Association. 2024 SIA Factbook. Washington DC: SIA; 2024. Available from: https://www.semiconductors.org/resources/2024-sia-factbook/
14. Beyne E. The rise of the 3D system—how chiplets and heterogeneous integration expand semiconductor capabilities. In: IEEE International Electron Devices Meeting (IEDM); 2021 Dec 11-15; San Francisco, CA. Piscataway: IEEE; 2021. p. 2.1.1-2.1.7. doi: 10.1109/IEDM19574.2021.9720526
15. Kim S, Lee S, Cha SW, Cho K, Park B. Hybrid bonding technology for advanced 3D-IC integration. J Electron Mater. 2023;52(4):1987-96. doi: 10.1007/s11664-023-10247-8
16. Green C, Kottke P, Fedorov A, Dede EM. Experimental characterization of manifold microchannel coolers for 3D-stacked chips. IEEE Trans Compon Packag Manuf Technol. 2020;10(12):1934-41. doi: 10.1109/TCPMT.2020.3026895
17. Lau JH. Fan-out wafer-level packaging for heterogeneous integration. IEEE Trans Semicond Manuf. 2021;34(1):107-26. doi: 10.1109/TSM.2020.3042828
18. Chen NC, Liao B, Chen LC. TSMC InFO (wafer level integrated fan-out) technology. In: Proceedings of the 66th IEEE Electronic Components and Technology Conference; 2016

May 31–Jun 3; Las Vegas, NV. Piscataway: IEEE; 2016. p. 1-6. doi: 10.1109/ECTC.2016.54

19. Prismark Partners. Panel-Level Packaging: Market and Technology Outlook 2024-2029. Cold Spring Harbor: Prismark; 2024.

20. US Department of Commerce. CHIPS Program Office: National Semiconductor Technology Center Concept Paper. Washington DC: DoC; 2023. Available from: https://www.nist.gov/system/files/documents/2023/02/28/NSTC-concept-paper-2023.pdf

21. Defense Advanced Research Projects Agency. CHIPS Program Overview. Arlington: DARPA; 2023. Available from: https://www.darpa.mil/program/chips

22. Defense Advanced Research Projects Agency. Electronics Resurgence Initiative 2.0 Program Announcement. Arlington: DARPA; 2022. Available from: https://www.darpa.mil/work-with-us/eri

23. Deloitte Insights; Semiconductor Industry Association. Chipping Away: Assessing and Addressing the Labor Market Gap Facing the US Semiconductor Industry. Washington DC: SIA; 2023. Available from: https://www.semiconductors.org/chipping-away/

24. IPC International. Advanced Packaging Substrate Market Report 2024. Bannockburn: IPC; 2024. Available from: https://www.ipc.org/ipc-advanced-packaging

25. Defense Microelectronics Activity. Trusted Foundry Program Overview. McClellan Park: DMEA; 2024. Available from: https://www.dmea.osd.mil/trustedic.html

26. Bureau of Industry and Security. Export Controls on Advanced Computing and Semiconductor Manufacturing Items. Fed Regist. 2022;87(200):62180-211. doi: 10.1357/bis.2022.87.200

27. Allen GC. Choking Off China's Access to the Future of AI. Washington DC: Center for Strategic and International Studies; 2022. Available from: https://www.csis.org/analysis/choking-chinas-access-future-ai

28. National Security Commission on Artificial Intelligence. Final Report. Washington DC: NSCAI; 2021. Available from: https://www.nscai.gov/wp-content/uploads/2021/03/Full-Report-Digital-1.pdf

29. Krinner S, Storz S, Kurpiers P, Magnard P, Heinsoo J, Riu R, et al. Engineering cryogenic setups for 100-qubit scale superconducting circuit systems. EPJ Quantum Technol. 2019;6(1):2. doi: 10.1140/epjqt/s40507-019-0072-0.

30. Schuman CD, Kulkarni SR, Parsa M, Mitchell JP, Date P, Kay B. Opportunities for neuromorphic computing algorithms and applications. Nat Comput Sci. 2022;2(1):10-9. doi: 10.1038/s43588-021-00184-y

31. Stojanovic V, Ram RJ, Popovic M, Lin S, Moazeni S, Wade M, et al. Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes. Opt Express. 2018;26(10):13106-21. doi: 10.1364/OE.26.013106.

32. Oxley TJ, Opie NL, John SE, Rind GS, Ronayne SM, Wheeler TL, et al. Minimally invasive endovascular stent-electrode array for high-fidelity, chronic recordings of cortical neural activity. Nat Biotechnol. 2016;34(3):320-7. doi: 10.1038/nbt.3428.